

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

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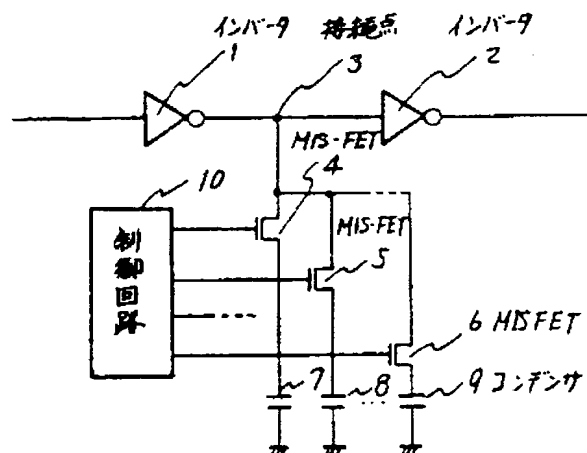
APPLICATION DATE : 12-04-85  
APPLICATION NUMBER : 60077833

APPLICANT : NEC IC MICROCOMPUT SYST LTD;

INVENTOR : TOBA TSUNEO;

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TITLE : SEMICONDUCTOR INTEGRATED  
CIRCUIT



ABSTRACT : PURPOSE: To attain change in the delay time even for a completed IC by connecting plural capacitors in parallel with an output section of an inverter via a transfer gate respectively and controlling each transfer gate.

CONSTITUTION: A transfer gate comprising MISFETs 4, 5, 6 and capacitors 7, 8, 9 connected in series with each transfer gate are connected between a common potential point and a connecting point 3 of inverters 1, 2 comprising MISFETs. A gate voltage is given to each gate of the MISFETs 4, 5, 6 from a control circuit 10. Since the capacitance value is adjusted depending on the number of the MISFETs 4, 5, 6 turned on by the control circuit 10, the time constant is changed to realize a delay circuit whose delay time is changed.

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